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ABSTRACT OF THE DISCLOSURE:

A data reproduction device including a CPU for reading out data from a memory card having a controller mounted thereon and a DSP for giving the read data required processing. The controller of the memory card is constructed such that an active mode is set for reading out the data under the current consumption of a first current value in response to memory access, and thereafter a standby mode automatically follows for waiting for next memory access under the current consumption of a second current value. The CPU reads out the data intermittently from the memory card at a first bit rate, and store the data to a buffer. The data stored in the buffer is read out at the second bit rate lower than the first bit rate, and supplied to the DSP.